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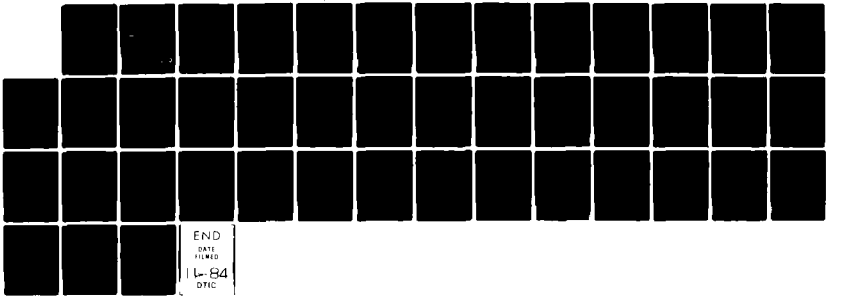

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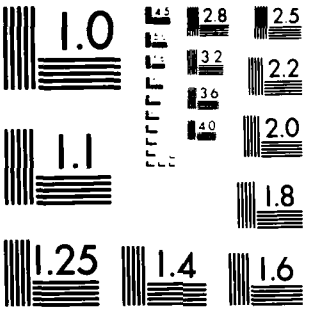

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A TOTAL DOSE CHARACTERIZATION OF FIVE COMMERCIAL ANALOG MULTIPLEXERS

1Lt Mark R. Ackermann

July 1984

Final Report

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AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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This report contains total dose radiation test data of five commercial grade analog multiplexers. Electrical parameter response data is provided and probable causes of failure are discussed.

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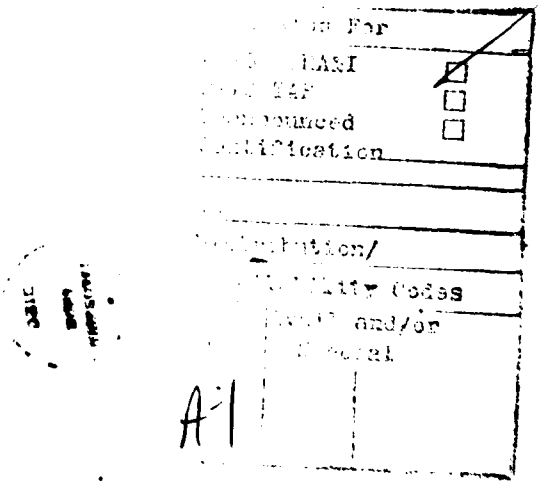

FIGURES

FIGURES (Concluded)

I. INTRODUCTION

Electronic components in satellite systems must be capable of surviving the high doses of ionizing radiation received during a space flight. Some devices are inherently insensitive to ionizing radiation while others suffer great shifts in their electrical operating characteristics after receiving comparatively small doses. For prolonged space flight, these sensitive devices must be shielded to reduce the doses received, but the shielding adds weight which increases launch costs. Many times manufacturers produce special radiation hardened components but these too are costly. Since current satellite radiation shielding is employed at the subsystem or box level, it is possible the heavy shielding required for a few soft components will provide sufficient protection to replace some of the costly radiation hardened components with commercial grade substitutes. This can be done, provided the commercial components are not overly sensitive to radiation.

Analog multiplexers may be candidate components for replacement with commercial equivalents since they appear in several satellite systems. Some manufacturers supply radiation hardened devices for space use but these devices are available in only a limited number of configurations. Many companies produce commercial grade analog multiplexers in a variety of processes and configurations, but these devices are not advertised to be radiation hard. The problem is to find those commercial components which have some natural radiation hardness.

Early commercial analog multiplexers suffered from poor electrical performance and were often prone to latch-up and possible burnout (Ref. 1). Some of these devices were little more than digital multiplexers adapted for use with analog signals. Newer analog multiplexer designs feature greatly improved electrical performance and several novel processing techniques the manufacturers have incorporated to prevent latch-up. Many of these novel features are similar to radiation hardened component designs. It seems reasonable to question whether or not some of the new analog multiplexers would have the required radiation hardness for use in space systems.

This report states the results of a study which compared the total gamma dose hardness of five commercial grade analog multiplexers and discusses possible failure mechanisms.

II. THE ANALOG MULTIPLEXER

DEVICE CONFIGURATION AND TECHNOLOGY

The five commercial grade analog multiplexers chosen for this study were the Harris HI-506A-5, the Siliconex DG506, the Fairchild F4067B, the Motorola MC14051, and the National LF11508. This selection includes CMOS and bipolar components and contains both 8- and 16-channel devices. Additionally, the selected CMOS components represent four different processes. Detailed information on each device is provided as follows.

The Harris HI-506A-5 is a 16 channel device fabricated in dielectrically isolated (DI) CMOS with built-in overvoltage protection diodes on all inputs. The DI process eliminates latch-up problems caused by parasitic four-layer devices by isolating each MOSFET in a well of silicon dioxide (SiO_2). Beneath the SiO_2 insulator well is a polycrystalline silicon substrate. Figure 1 shows a cross-sectional view of a dielectrically isolated CMOS transistor pair.

Critics of the DI process claim that it is rather costly due to increased processing steps and that it produces analog switches with higher on resistances (Ref. 1). The DI process is more costly but it is claimed that the smaller chip size allowed by this technique allows for greater yield, thereby offsetting the increased cost. As for the channel on resistances, there is no question. The DI CMOS channels have resistances about five times that of other CMOS processes.

The Siliconex DG506 is a pin-for-pin functional equivalent of the HI-506-5 16-channel analog multiplexer. Siliconex processes the device in their own special latch free CMOS process which features a p+ layer buried beneath the p- wells. This buried layer is intended to prevent latch-up by decreasing the npn - pnp beta product to less than one. A cross-sectional view of the buried layer construction is shown in Figure 2.

The Fairchild F4067B is a 16-channel device fabricated in Fairchild's Isoplaner C-CMOS technology. Conventional silicon gate CMOS processes utilize diffused n+ and p+ channel stops between adjacent devices and at the edges of the p well as shown in Figure 3a. The Fairchild Isoplaner process utilizes local oxidation isolation in place of the channel stops as shown in Figure 3b. The locally oxidized channel stops are easier and cheaper to fabricate than

the elaborate upside down DI process. Additionally, Fairchild claims they reduce chip size by an average of 35 percent thereby allowing for more die on each wafer. Fairchild advertises the Isoplaner CMOS has greater noise immunity than conventional CMOS products.

The Motorola MC14051 is an 8-channel analog multiplexer from the common 4000 series CMOS family. This device features large geometry components and protection diode circuitry on all inputs. These components offer surprisingly good performance, they are cheap, readily available, and are produced with a multiple of second sources.

The National LF11508 is the final multiplexer examined in this study. The LF11508 is an 8-channel device fabricated with bipolar logic and drivers and JFET transistors for the actual analog channels. National chose to avoid the latch-up problem altogether by avoiding CMOS.

National calls the combined bipolar and JFET process a BiFet technology. Figure 4 shows a cross-sectional view of a BiFet device. This technology offers a sound alternative to CMOS devices but features a slightly reduced electrical operating range for the analog signal and dissipates more power than CMOS alternatives.

Regardless of manufacturer, design and process technology, the analog multiplexer by itself is a rather interesting device since it combines both digital and analog functions on a single chip. The digital portion consists of the chip select and digital decoding logic. The analog portion consists of the analog transfer gates. While not as complex as an analog to digital converter, the analog multiplexer is more interesting to test since the analog portions may be accessed somewhat independently of the digital logic. A function block diagram of an analog multiplexer is presented in Figure 5.

THE ANALOG TRANSFER GATE

The design of a MOSFET analog transfer gate deserves some attention. Ideally, the user of an analog transfer gate would like for the device to have infinite off-resistance and an on-resistance which is low and constant over the full analog operating range. Additionally, a circuit capable of driving both low and high impedance loads which has both CMOS and TTL compatability is desirable, but not easy to design.

The simplest form of a transfer gate is a single p- or n-channel MOSFET. Figure 6 shows an n-channel MOSFET with the gate, V_g, biased at +10 V and the p-type substrate held at ground. Under most combinations of drain and source biases, with V_g = 10 V, the transistor will be in the ON condition and either a partial or complete conducting channel will exist. Applying a bias V_d to the drain will produce a voltage at the source, V_s, which will depend upon the load R_L, and the channel resistance. The channel resistance, however, depends upon V_d, V_g, V_s, and the substrate bias, V_{ssp}. Before examining the channel resistance in detail, it should be mentioned that most analog transfer gates are intended to be bidirectional and, hence, the source and drain regions are identical. The choice of drain and source is arbitrary.

To examine the resistance of a MOSFET conducting channel, start with a biased transistor (Fig. 6) with the source tied to ground, i.e., $V_s = 0$. When the drain voltage is less than the saturation drain voltage, $V_d < V_{dsat}$, the FET is operating in the linear region where the channel conductance is constant and given by

$$g = \frac{\partial I_d}{\partial V_g} = \frac{Z\mu_n C_o}{L} (V_g - V_t) \qquad (1)$$

for $V_g > V$

$V_{dsat} = V_g - V_t$

The linear region channel resistance, R_c, is given by

$$R_c = 1/g \qquad (2)$$

A typical p-channel MOSFET may have a linear region channel conductance on the order of 10^{-3} S, giving a resistance of 1000 Ω (Ref. 4).

When $V_d > V_{dsat}$, the FET is operating in the saturation region. In this mode of operation, the channel dislays the characteristics of a high impedance load, as large changes in V_d produce only small changes in the drain current, I_d. In the saturation region, the channel conductance takes on the complex form of

$$g_{sat} = \frac{Z\mu_n C_o (zK_{s\,o}/qN_m)^{1/2}}{4L^2 (V_d - V_{dsat})^{1/2}} \qquad (3)$$

for $V_d > V_{dsat}$

Again, the channel resistance is given as

$$R_c = 1/g_{sat} \tag{4}$$

Note that g_{sat}, and the saturation region channel resistance is not constant but instead depends upon V_d. Such a behavior is not desirable for an analog transfer gate. Figure 7 shows the qualitative relations between V_d and I_d, and between V_d and R_c for an n-channel MOSFET with constant $V_g > V_t$, operating in the common source mode. All of the equations are valid for a p-channel device with appropriate changes in polarity.

Next, look at an n-channel MOSFET biased as in Figure 6 with the source connected through a high load resistance, R_L, to ground. In this case, an applied drain voltage, $V_d < V_{dsat}$, will cause a current to flow through the channel and the load resistance to ground. If R_L is sufficiently large, (i.e., at least on the order of the channel resistance) it will be responsible for a large percentage of the voltage drop between V_d and ground. Hence, the source voltage V_s will differ significantly from ground. Such an applied source to substrate bias will shift the transistor threshold voltage, V_t. The resulting threshold voltage V_t' is given by (Ref. 5)

$$V_t' = V_t \pm \left(\frac{X_o}{K_{ox}\epsilon_o}\right)\left(2K_s\epsilon_o q N_m\left(|2\phi_f + V_s|\right)\right)^{1/2}\left(\left(\frac{2\phi_f + V_s}{2\phi_f}\right)^{1/2} - 1\right) \tag{5}$$

where

for n-channel devices the + is used and

V_{ssp} = ground

$V_s > V_{ssp}$

for p-channel devices the - is used and

V_{ssn} = ground

$V_s < V_{ssn}$

The change in the threshold voltage, $\Delta V_t = V_t' - V_t$, is positive for n-channel devices and negative for p-channel devices. Such changes cause MOSFET channel resistances to increase; hence, the channel resistance is a function of the loading condition and the analog signal. Such a behavior is not desirable for analog transfer gates.

To compensate for some of these problems, manufacturers designed analog transfer gates which use both n- and p-channel transistors. When connected in parallel and biased as shown in Figure 8, the n- and p-channel enter their respective saturation regions at opposite ends of the analog signal range. This configuration produces an analog transfer gate whose resistance is more slowly varying than a single MOSFET transfer gate. Source to substrate biases still produce threshold voltage shifts in the individual transistors, but again, the n- and p-channel transistors are affected at opposite ends of the analog signal range and the effects on the channel resistance tend to partially offset each other.

The complimentary pair analog transfer gates function better at the extreme ranges of the analog signal than a single n- or p-channel transfer gate, but the channel resistances are not perfectly constant and still suffer from changes in the load resistance. To further compensate for such effects, manufacturers have adopted designs where the analog signal is processed and used to vary the substrate biases on the actual transfer gate transistors. Such designs are more involved and a detailed understanding of their operation is not necessary for this report.

RADIATION EFFECTS

Traditionally, bipolar devices have been extremely resistant to ionizing radiation. Some recent bipolar devices, such as those using oxide isolation or those with small geometries, are proving to have significant total dose problems related to effects at the SiO_2 interface or the device surface. The National LF11508 analog multiplexer does not use small geometries or oxide isolation and is not expected to suffer significant total dose problems.

In MOSFETs, ionizing radiation produces electron-hole (ion) pairs in the SiO_2 insulator. The electrons are extremely mobile and either diffuse or are rapidly swept out by any electrical field. The holes, being much less mobile, move more slowly. Eventually a large portion of the holes reach the $Si\text{-}SiO_2$ interface where they are either trapped or aid in the formation of additional fast surface states (known as interface states).

The effect of positive charge in the oxide of a MOSFET is to produce a negative threshold voltage shift in both n- and p-channel devices. Interface

states display a gate voltage dependent effect on MOSFETs. In general, the n-channel device will be affected primarily by acceptor interface states. When the n-channel gate is biased positive with respect to the p- well, the acceptor interface states are negatively charged and produce positive shifts in the threshold voltage. The p-channel device is primarily affected by donor interface states which are positively charged when the gate is biased negative with respect to the n-type substrate. The donor interface states produce a negative shift in the p-channel threshold voltage.

Figure 9 shows qualitatively the effects of an ionizing radiation on the threshold voltages of n- and p-channel MOSFETs. Such general threshold voltages would be seen from transistors operated in the common source mode with both the p-well and n-substrate grounded. The specific effects of different dose rates during irradiation, bias conditions during irradiation, and annealing are not considered in this discussion. At this time we are concerned only with the general nature of the threshold voltage shifts. It is possible to obtain data such as shown in Figure 9.

Line D in Figure 9 represents the typical effect of radiation on the p-channel threshold voltage. At early times the shift appears linear with dose. This occurs while positive charge is trapping at the interface. At later times (on the order of 1000 s) the donor interface states begin forming there by adding to the negative shift. From Equations 1 and 2, it is seen that a negative shift in the threshold voltage increases the linear region channel resistance of a p-channel MOSFET. If the threshold voltage shifts negative too far, the channel conductance will approach zero for a given gate voltage. Hence, the p-channel portion of the analog transfer gate will no longer function. This failure mode is rarely seen since the difference between V_g and V_t for the p-channel FET is greater than the difference between V_t and ground for the n-channel FET. Hence, the n-channel transistor usually experiences failure first.

The behavior of the n-channel device is somewhat more complicated since charge trapping at the interface causes a negative shift, while the acceptor interface states cause a positive shift. The threshold voltage shift shown in line A of Figure 9 represents the worst case for the analog transfer gate. In this situation, the n-channel threshold voltage has gone negative with respect

to the p- well bias. With a negative threshold voltage, the n-channel member of the transfer gate cannot be turned off; hence, the analog channel conducts even when turned off.

Line B of Figure 9 represents another possible way in which the n-channel threshold voltage may behave. In this case, the formation of the interface states produced a significant positive shift which partially compensates for the negative shift caused by the trapped charge. Line C of the figure shows a similar situation, but in this case the threshold voltage never crosses the zero mark and finally exhibits a net positive shift.

Radiation hardened CMOS FETs in a low dose rate environment, such as space, will likely exhibit threshold voltage shifts similar to those depicted by lines C and D of Figure 9. Most commercial grade CMOS components will act similar to lines A and D. This behavior tends to increase the p-channel resistance and decrease the n-channel resistance, which in effect decreases the transfer gate resistance at the low end of the analog signal range, and increases resistance at the high end. With increasing total dose, we should expect to see an overall change in the analog transfer gate resistance combined with a change in the resistance slope as a function of the analog input signal.

III. ELECTRICAL CHARACTERIZATIONS

PARAMETER MEASUREMENTS

To determine the nature and effect of the damage produced by ionizing radiation, a variety of electrical parameters were measured on each device. Although many electrical parameters could have been checked, for reasons of practicality, only six were examined. The particular tests were chosen to measure the parameters which seemed most critical from the system design point of view. Of the six measurements made, four were intended to examine the characteristics of the analog channel, one measurement pertained to the chip as whole, while the last was intended mainly to examine the digital decode logic. The details of each test are as follows.

First is the measurement of the device supply currents. The negative and positive supply currents of all devices were measured both while the device was in a standby mode, and while having its digital channel select lines exercised by a square wave. The square wave frequency was adjusted until the current read a maximum. The current was measured as the voltage drop across a precision 1 Ω resistor.

In general, device supply current measurements are made as a gross measure of increased transistor leakage. Additionally, increased device supply current is of critical concern to system designers.

To observe degradations in transistor switching speed, and to examine the digital portions of the devices, the maximum control frequency of selected analog channels was measured. The specific technique for this test was derived from the test circuits section of the Motorola MC14051 specification sheet. The test circuit is shown in Figure 10. The Motorola specification sheet shows the supply voltage being applied to the analog input of the channel in question. Meanwhile a square wave is applied to some combination of the digital channel control inputs. The common analog output is dropped across a suitable load resistance and observed on an oscilloscope. The square wave is increased in frequency until the analog output amplitude is equal to $(V_{DD} - V_{EE})/2$. What the specification sheet does not indicate is to connect

the analog input of channel number zero to V_{EE}. This connection is necessary since channel zero is selected when the square wave goes low. This oversight presents no problem if the device is being operated from a single power supply. If however, it is operated with positive and negative power supplies, this connection is essential. When the square wave goes low, if channel zero is not biased at V_{EE}, adjusting the control frequency until the analog output amplitude is $(V_{DD} - V_{EE})/2$, is meaningless.

Of the four devices in this test, only the Fairchild part was operated from a single power supply. On the Fairchild part, all analog inputs, except for that of the channel in question, were grounded during the control frequency test. For the other four components, the channel addressed by the square wave was connected to V_{DD}, the zero channel was connected to V_{EE}, and all other channel inputs were grounded.

The load resistance used for this test for each of the devices was determined from the device specification sheets. These load resistances were as follows:

Harris HI-506A-5	1 kΩ
Siliconex DG506	1 kΩ
Fairchild F4067B	1 kΩ
Motorola MC14051	1 kΩ
National LF11508	10 MΩ

The remaining four parameters were measured to characterize the analog portion of the multiplexer. The first of these tests was an analog bandwidth measurement. It was assumed that the devices had no problem passing slowly varying analog signals, so the test consisted of measuring the maximum passable analog frequency. Once again, the test circuit came from the MC14051 data sheet and is shown in Figure 11. The test consists of digitally selecting a channel, applying a $(V_{DD} - V_{EE})/2$ sine wave to the channel input, and adjusting the frequency until the output amplitude is at the -3 dB point. This frequency is arbitrarily defined as the channel bandwidth. The load resistances used for this test are identical to those used for the control frequency test.

The next test measured the analog channel resistance. For this test, a particular channel was selected and a given voltage was applied to the analog input. The channel output was connected to ground through a 1 kΩ precision resistor. The channel resistance was computed after measuring the voltage drop across the 1 kΩ resistor.

For all the devices tested, the analog input voltage was started at V_{EE} and stepped across the entire analog operating range in one volt increments. At each stop, the channel resistance was computed. From these data, the average channel resistance and the slope of the resistance-voltage function was computed and recorded.

The next test was intended to determine if an analog channel was suffering from any voltage cut-off at the extreme limits of the operating range and to measure any offset voltages. The test circuit and technique are rather simple. First an analog channel was selected, a programmable power supply was connected to the analog input, and a 10 MΩ input digital voltmeter was connected to the output. The power supply was programmed to begin at V_{EE} and step its way up to V_{DD} in 1/4 V increments. At each step, the output voltage was recorded. From these data, the slope of the transfer function was computed along with the output voltage offset. A correlation coefficient for the line fit was also computed as a measure of linearity.

The final test was to measure any leakage through a channel which was not selected. This test was conducted identically to the first test except for the channel not being selected. The offset voltage measured by a 10 MΩ digital voltmeter provides the means of calculating the leakage current.

TEST EQUIPMENT

A large selection of test equipment was required to make the measurements previously described. Whenever possible, the measurements were automated using a Hewlett Packard HP-9825 experiment controller equipped with an IEEE-488 bus. It was not always possible to automate measurements due to the limited selection of IEEE-488 compatible instruments.

The tests which were automated include the channel resistance and leakage current measurement, and the linearity check. These tests required the experiment controller, a programmable power supply and digital voltmeter.

The remaining three tests were performed manually. The analog bandwidth measurement required a leveled output sine wave generator, an oscilloscope, and a frequency counter. Due to a problem with the sine wave generator and the inability to locate a substitute replacement with a leveled output, the analog bandwidth measurements were not performed on the Fairchild device.

The control frequency test required a square wave generator, a frequency counter, and an oscilloscope. At the time these tests were being performed, the only high frequency square wave generator available was a serial word generator. This word generator had a super fast rise time and produced a sharp square wave.

In addition to this equipment, numerous power supplies, voltmeters, and oscilloscope plug-ins were required. The make and model numbers of specific equipment items are presented below:

Hewlett Packard	HP-9825	Experiment Controller
Hewlett Packard	HP-5342A	Frequency Counter
Hewlett Packard	HP-5328A	Digital Voltmeter
Hewlett Packard	HP-6002A	Programmable Power Supply
Tektronix	SG-503	Sine Wave Generator
Tektronix	R7844	Oscilloscope

IV. RADIATION TEST PROCEDURES

All the total dose exposures were performed at the Air Force Weapons Laboratory (AFWL) Co^{60} Gamma Irradiation Facility. The AFWL source is a 5 kCi Co^{60} rod which was installed on 1 July 1978. The exposure cell consists of a 1500 sq ft room with a lead pig near the center. Approximately 50 coaxial cables are available for testing the devices during irradiation. The cables run up into the control room 130 ft away.

When in operation, the source rises out of the pig into a thin aluminum dustcover. Test devices are placed on a table near the dustcover. The dose received is controlled by varying the exposure length and distance from the source.

All exposures for the multiplexers were conducted between March and May of 1982. The dose rates were between 1 and 10 krads (Si)/min. The devices were characterized before irradiation and after certain total doses had been achieved. The intermediate characterization points for the different devices were not always the same due to fluctuations in the time available at the Co^{60} facility.

Each device type was tested in three different bias configurations. The first set of devices was exposed with the device at hard ground. All the pins of each device were tied to ground. In the next configuration, the device was connected to the appropriate power supplies, but all other pins were connected to ground. In the final configuration, the devices were in operation during the exposure. The zero channel input was connected to V_{EE}, one channel was connected to V_{DD}, the common analog output was connected across a 1 kΩ resistor to ground, and the digital control for the special channel was exercised with a 100 kHz square wave. All the remaining analog inputs were connected to ground. All the devices were removed from the test cell for characterization. This process took approximately 10 min so the effects of any annealing should be minimal.

V. RADIATION RESPONSE DATA

The results of the radiation testing proved to be interesting. In general, the devices responded as would be expected. The devices survived the longest when they were fully grounded, and died the fastest when biased but in standby. As expected, the bipolar device survived a 1 Mrad total dose and most of the CMOS devices died at much lower doses. And as expected, radiation caused the slope of the channel resistance versus analog voltage to increase slightly, but there were only slight shifts in the average channel resistance. There were, however, some surprises in the data.

The Motorola device responded as expected when biased active or in standby. The surprise was that when fully grounded, this device survived in excess of 1 Mrad. Another surprise was that the main failure mechanism of all the CMOS devices was operational failure of the digital decode logic. The analog portions of the device were only slightly affected by the radiation. The digital logic was expected to fail but it was hoped that it would survive long enough to see some parametric degradation of the analog characteristics.

The total dose failure points of the devices for the three test modes are presented in tabular form. For the fully grounded and standby devices, two doses are listed. The first dose is the last point at which the device was characterized and functional. The second dose listed is where the device was found to be dead. The actual failure point lies somewhere between these two values. For the devices irradiated while active, four doses are listed. The first two doses are for the active channel and the second two for a channel which was not being exercised. The two doses for each channel type are the same as previously mentioned for the grounded and standby devices.

GROUNDED DEVICES

DEVICE	LAST KNOWN FUNCTIONING	FOUND DEAD krads
HI-506A-5	100 krads	300
DG506	70 krads	100
F4067B	100 krads	300
MC14051	1 Mrad	---
LF11508	1 Mrad	---

STANDBY DEVICES

DEVICE	LAST KNOWN FUNCTIONING	FOUND DEAD krads
HI-506A-5	50 krads	100
DG506	3500 rads	5
F4067B	30 krads	70
MC14051	10 krads	20
LF11508	1 Mrad	---

ACTIVE DEVICES

	-----ACTIVE CHANNEL-----		----PASSIVE CHANNEL----	
DEVICE	LAST KNOWN FUNCTIONING	FOUND DEAD krads	LAST KNOWN FUNCTIONING	FOUND DEAD krads
HI-506A-5	100 krads	200	20 krads	50
DG506	7500 rads	15	7500 rads	15
F4067B	10 krads	30	10 krads	30
MC14051	50 krads	100	10 krads	20
LF11508	1 Mrad	---	1 Mrad	--

Figures 12 through 17 are plots of the standby supply currents versus total dose for the five device types. The active supply currents are not plotted due to greater uncertainty in these measurements. The action of adjusting the digital control frequency until the current measures a maximum leaves room for operator error. Measuring standby current, on the other hand, is a well defined procedure.

Figures 18 through 24 are plots of the normalized maximum digital control frequency versus total dose. The frequencies were plotted as a percentage of their initial value. Figures 18 and 19 are plots for the grounded and standby devices respectively. These plots feature all five device types. Figures 20 through 24 are plots for the devices when irradiated in an active mode. Each plot features only one device type but presents data for both the active and passive channels.

VI. CONCLUSIONS

Although the main function of an analog multiplexer is to switch analog signals, the primary failure mechanism seems to be in the digital control circuitry. Avoiding the controversy of new bipolar processes, the older bipolar process National multiplexer, as expected, was significantly more resistant to ionizing radiation than any of the commercially available CMOS components. Of the techniques to prevent latch-up employed by Harris, Siliconex, and Fairchild, the Harris dielectric isolation process clearly offers the greatest radiation survivability.

Of the five component types tested, only the Harris and National devices appear to have sufficient radiation hardness to even be considered for use in space. Both components, however, have their drawbacks too. The National device is somewhat power hungry and the radiation resistance of the Harris device is somewhat borderline in certain modes of operation.

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2. Fairchild CMOS data book, 1983.

3. National linear data book, 1980.

4. Grove, A. S., The Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc., New York, 1967.

5. Richman, P., MOS Field-Effect Transistors and Integrated Circuits, John Wiley and Sons, Inc, New York, 1973.

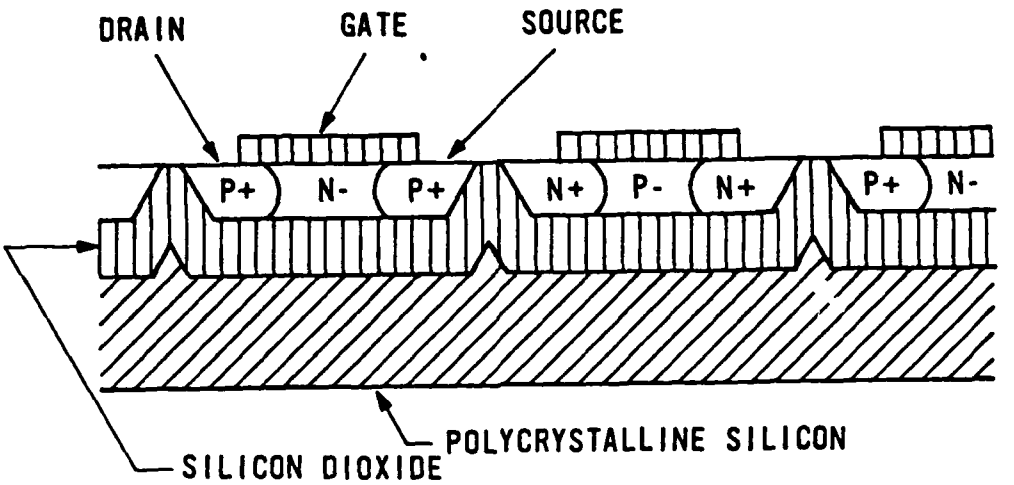


Figure 1. Cross-sectional view of a dielectrically isolated CMOS transistor pair (Ref. 1).

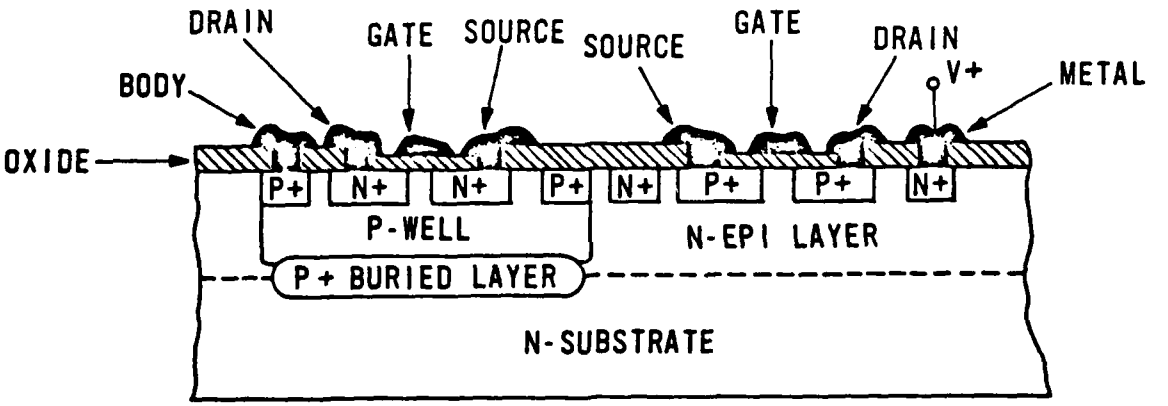


Figure 2. Cross-sectional view of the buried layer CMOS process used by Siliconex (Ref. 1).

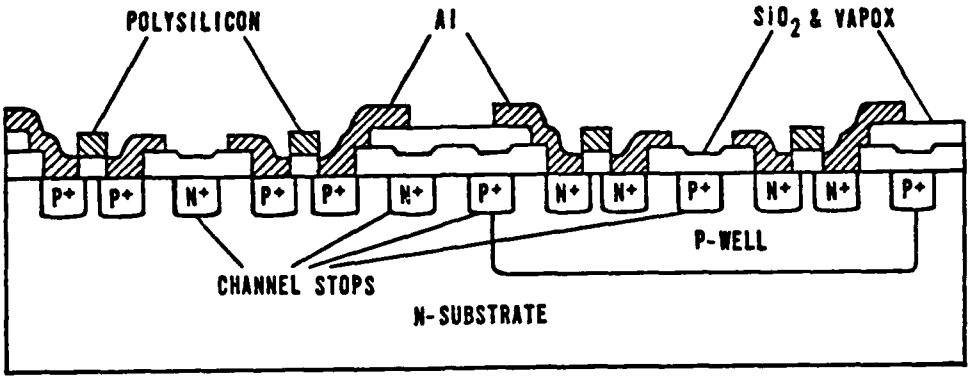


Figure 3a. Conventional CMOS utilizing diffused channel stops (Ref. 2).

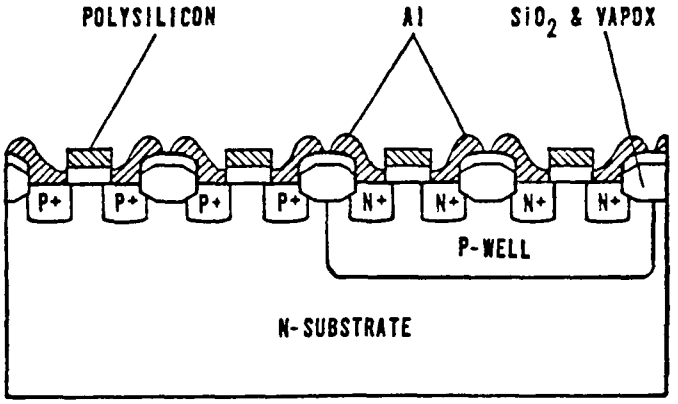


Figure 3b. The Fairchild Isoplaner C-CMOS process utilizing local oxide isolation in place of diffused channel stops (Ref. 2).

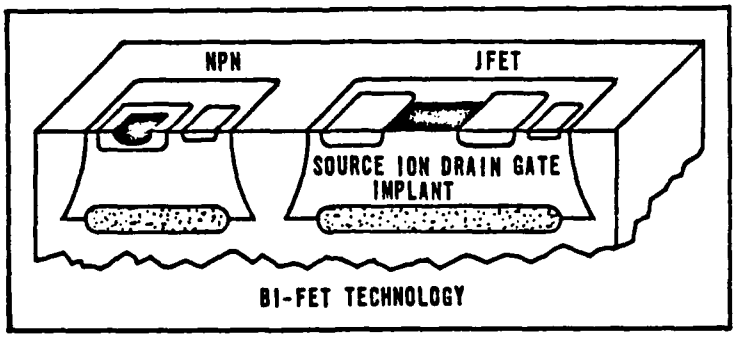


Figure 4. Cross-sectional view of the National BiFet process (Ref. 3).

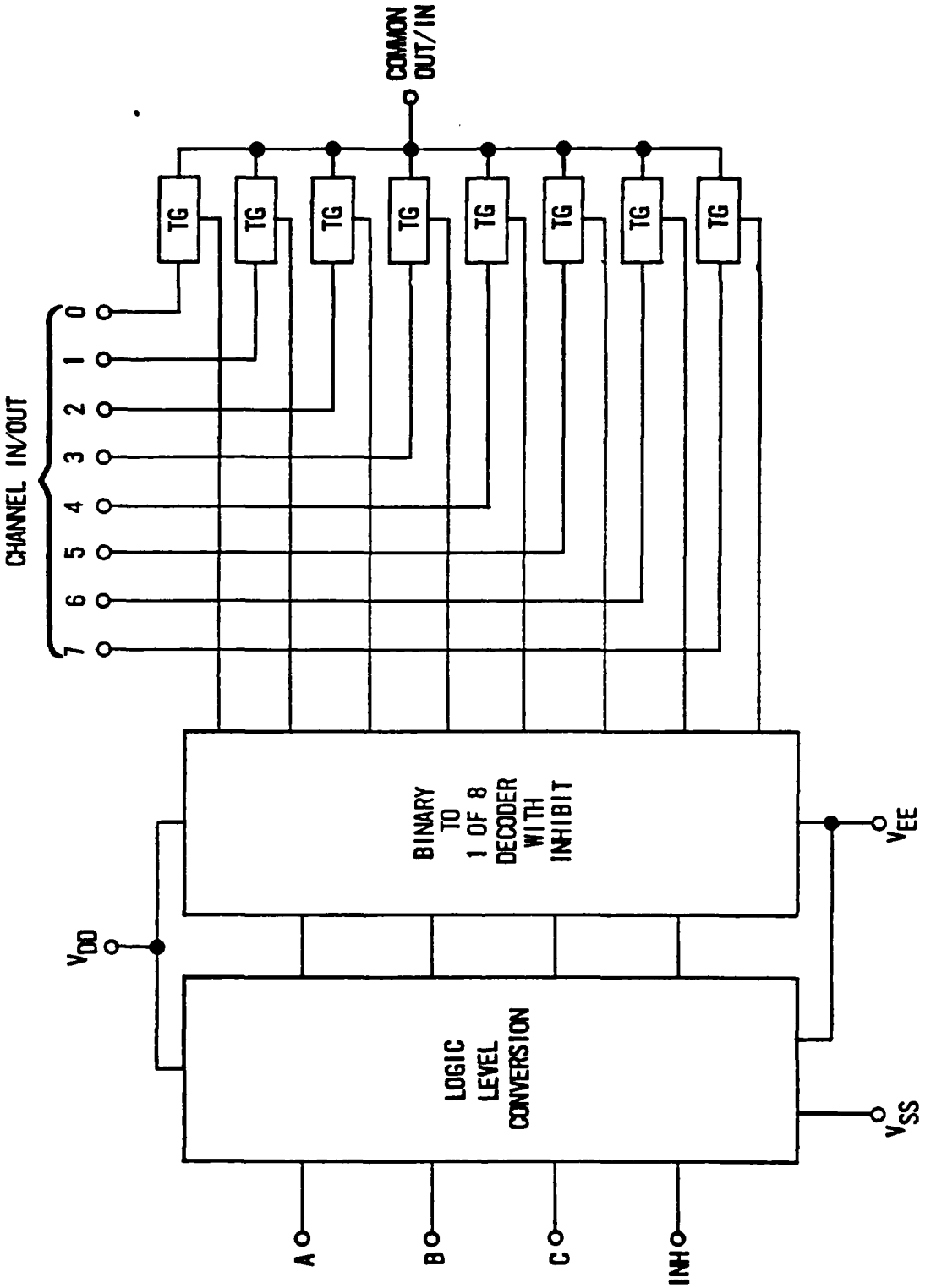


Figure 5. Analog multiplexer functional block diagram.

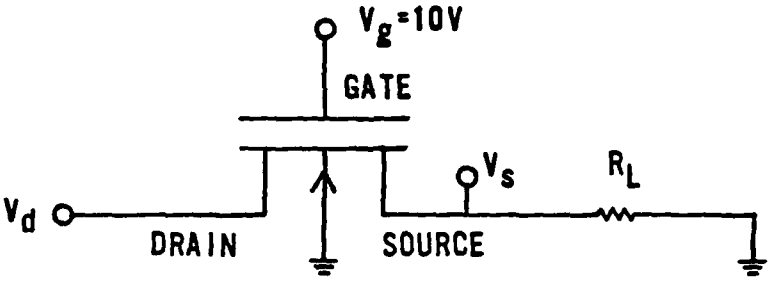
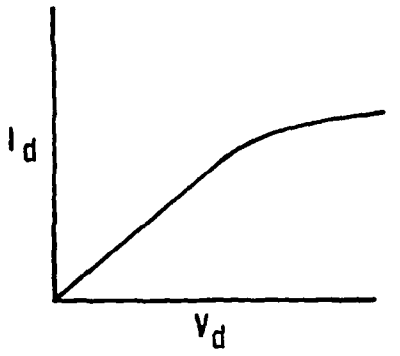


Figure 6. N-channel MOSFET analog transfer gate.



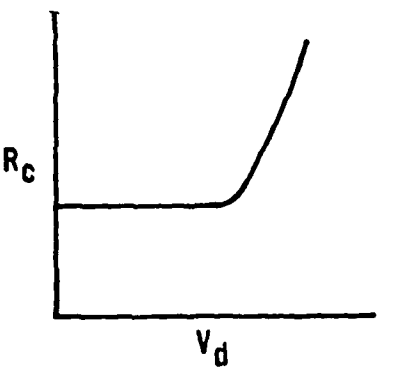


Figure 7. The qualitative relation between the drain voltage V and (a) the drain current I, and (b) the channel resistance R for an n-channel MOSFET.

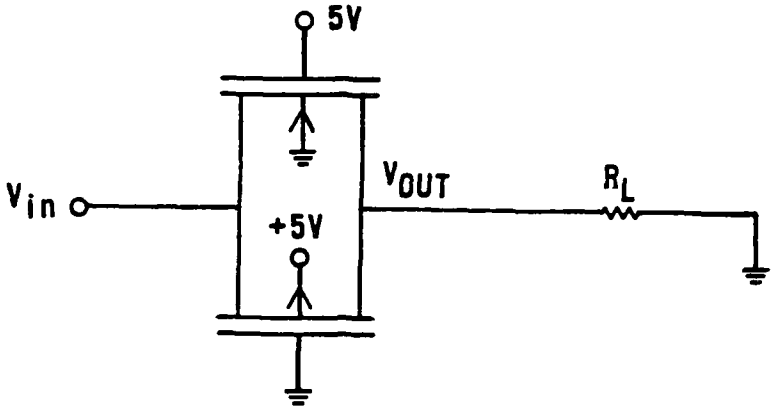


Figure 8. A CMOS analog transfer gate.

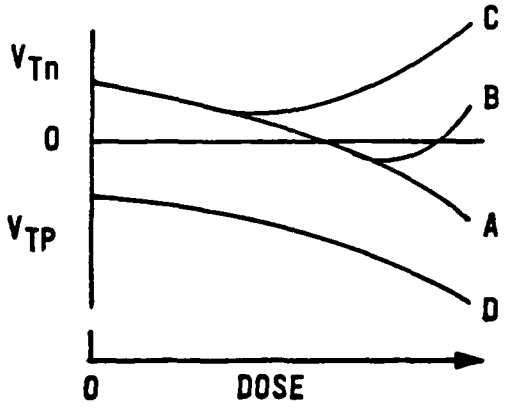


Figure 9. Possible n- and p-channel threshold voltages as a function of total absorbed dose.

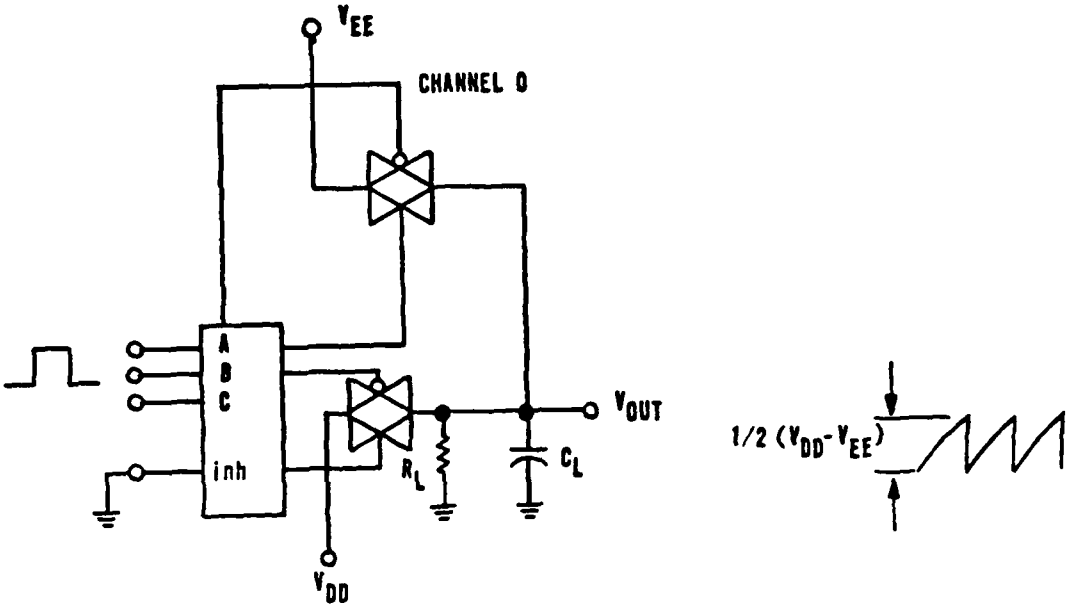


Figure 10. Maximum control frequency test circuit.

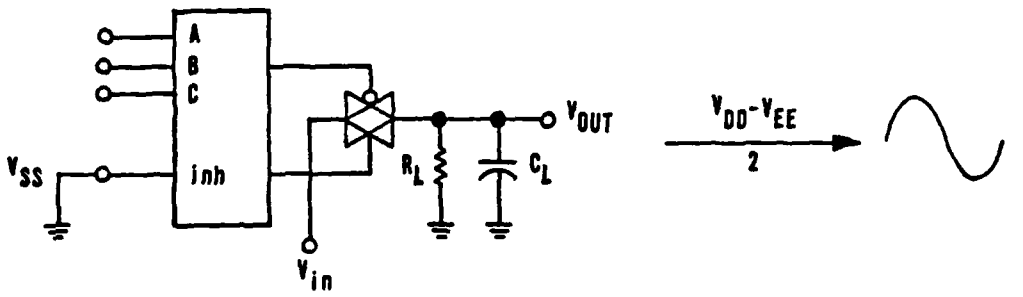


Figure 11. Analog bandwidth test circuit.

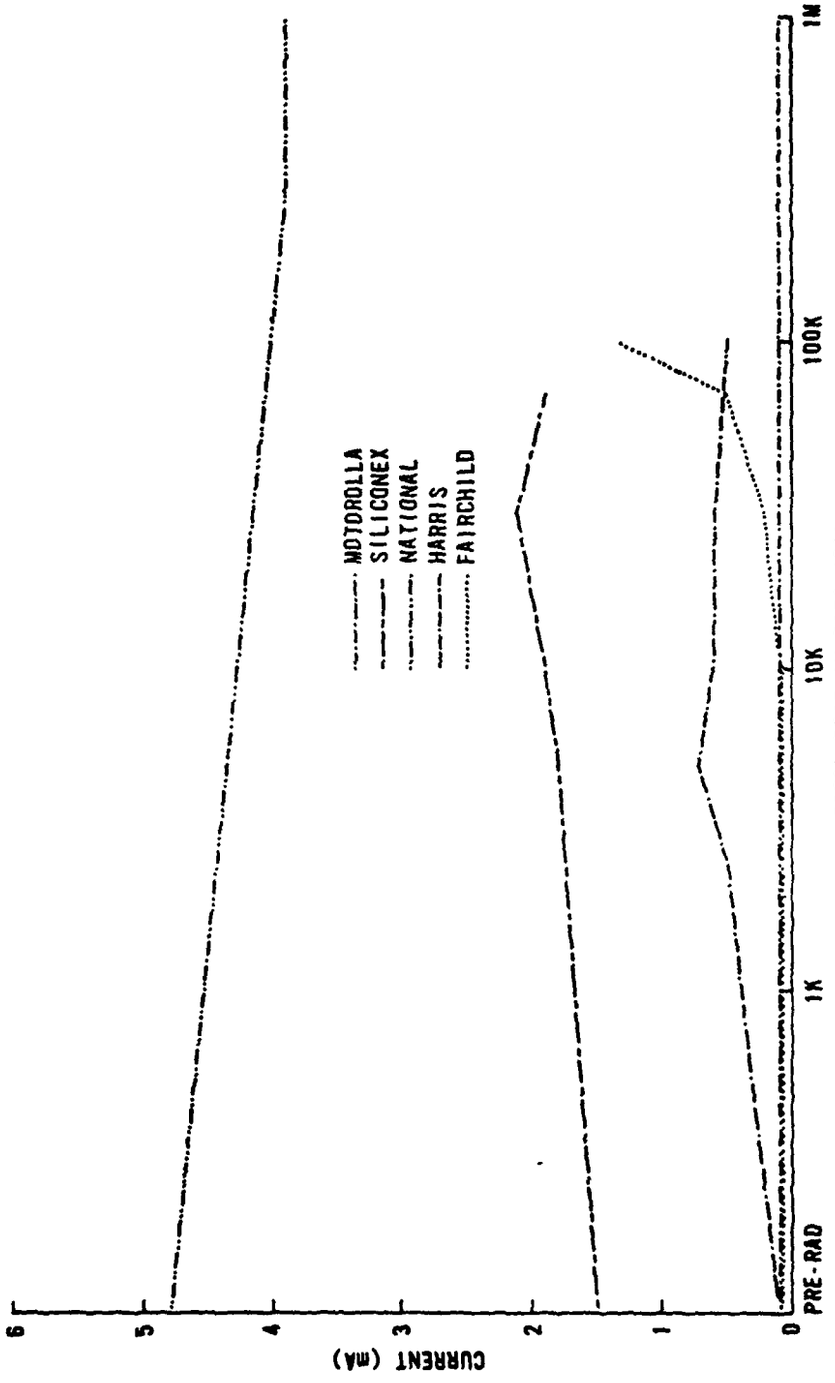


Figure 12. Positive standby supply current for devices irradiated while grounded.

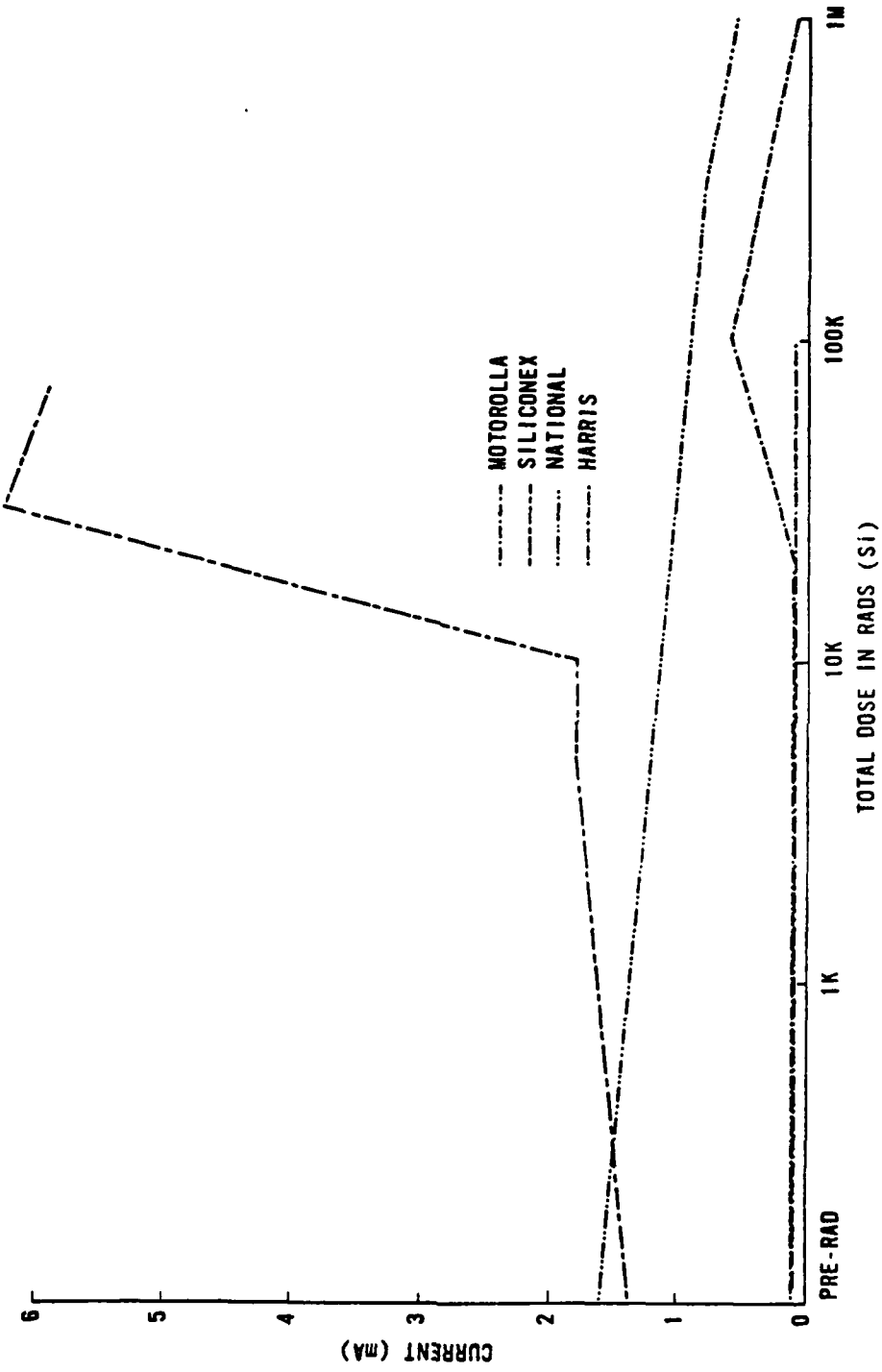


Figure 13. Negative standby supply current for devices irradiated while grounded.

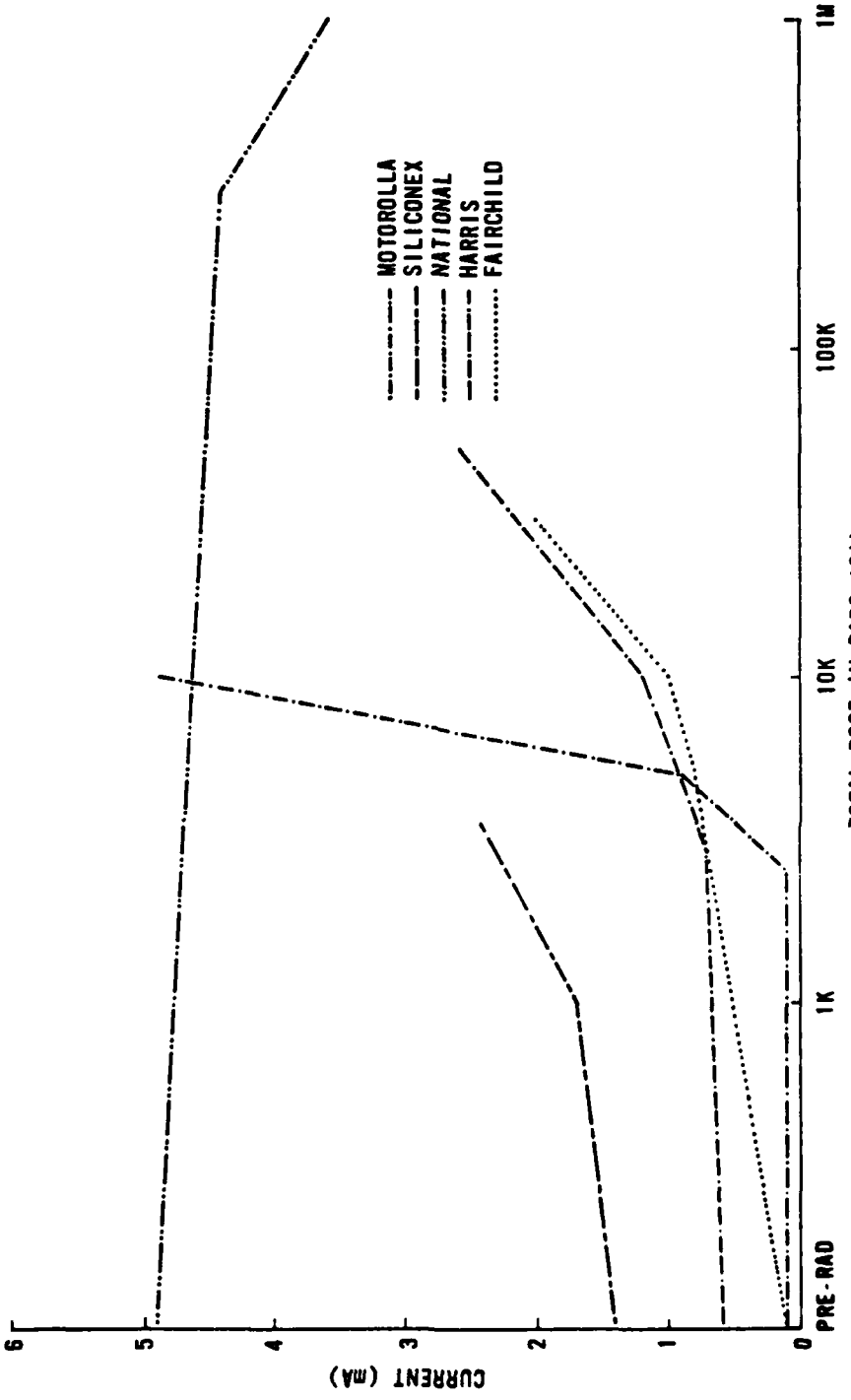


Figure 14. Positive standby supply current for devices irradiated while statically biased.

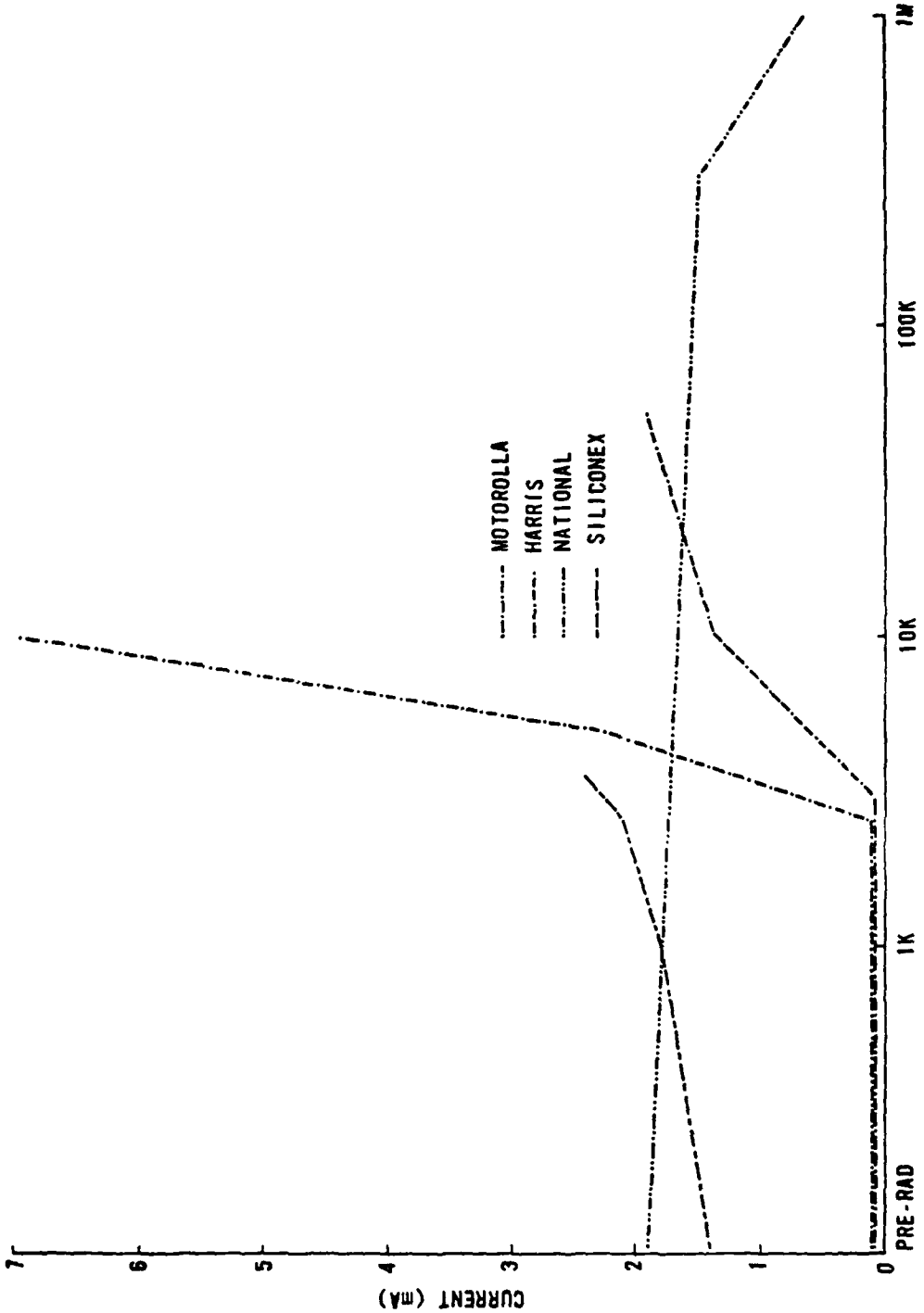


Figure 15. Negative standby supply current for devices irradiated while statically biased.

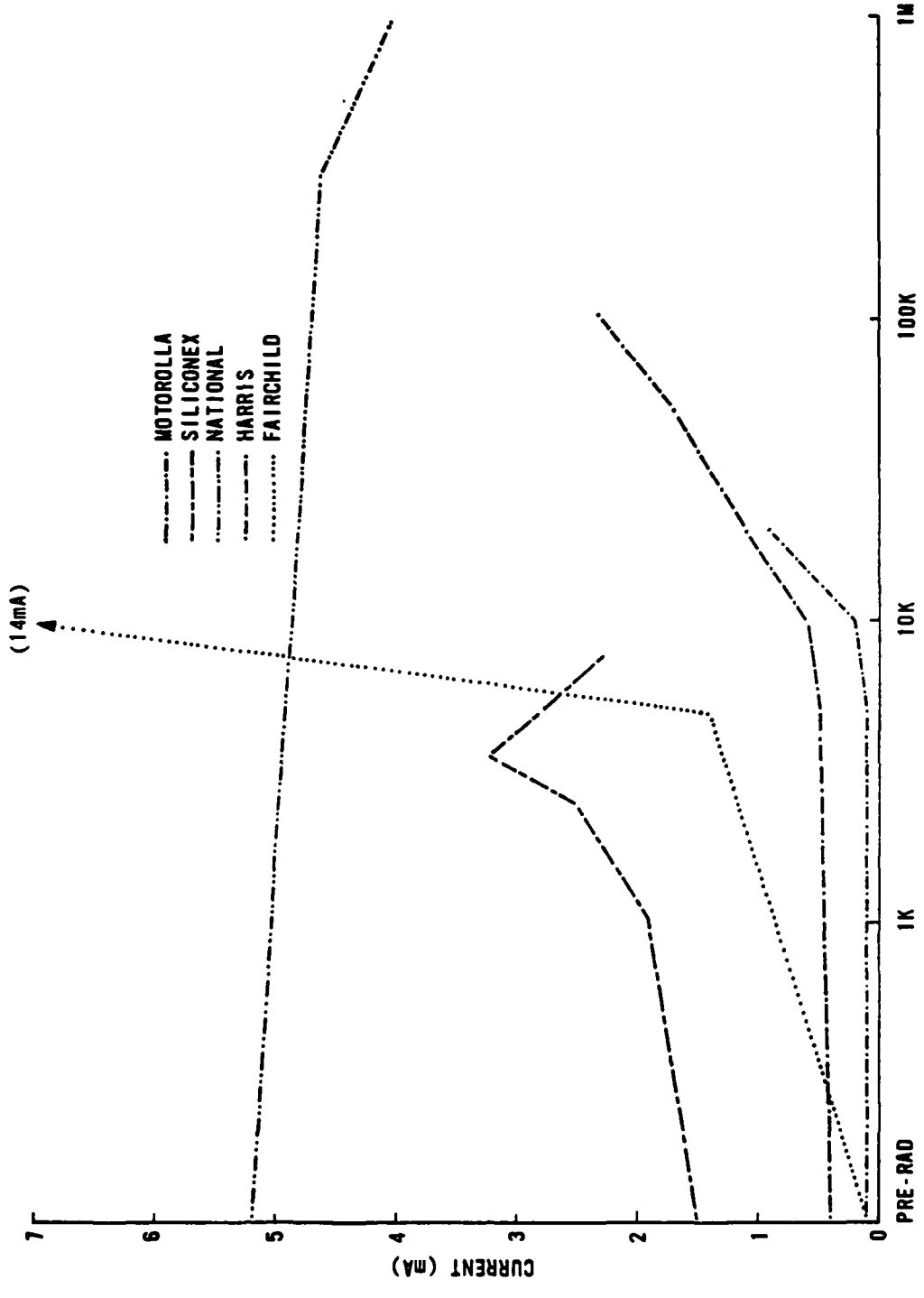


Figure 16. Positive standby supply current for devices irradiated while actively biased.

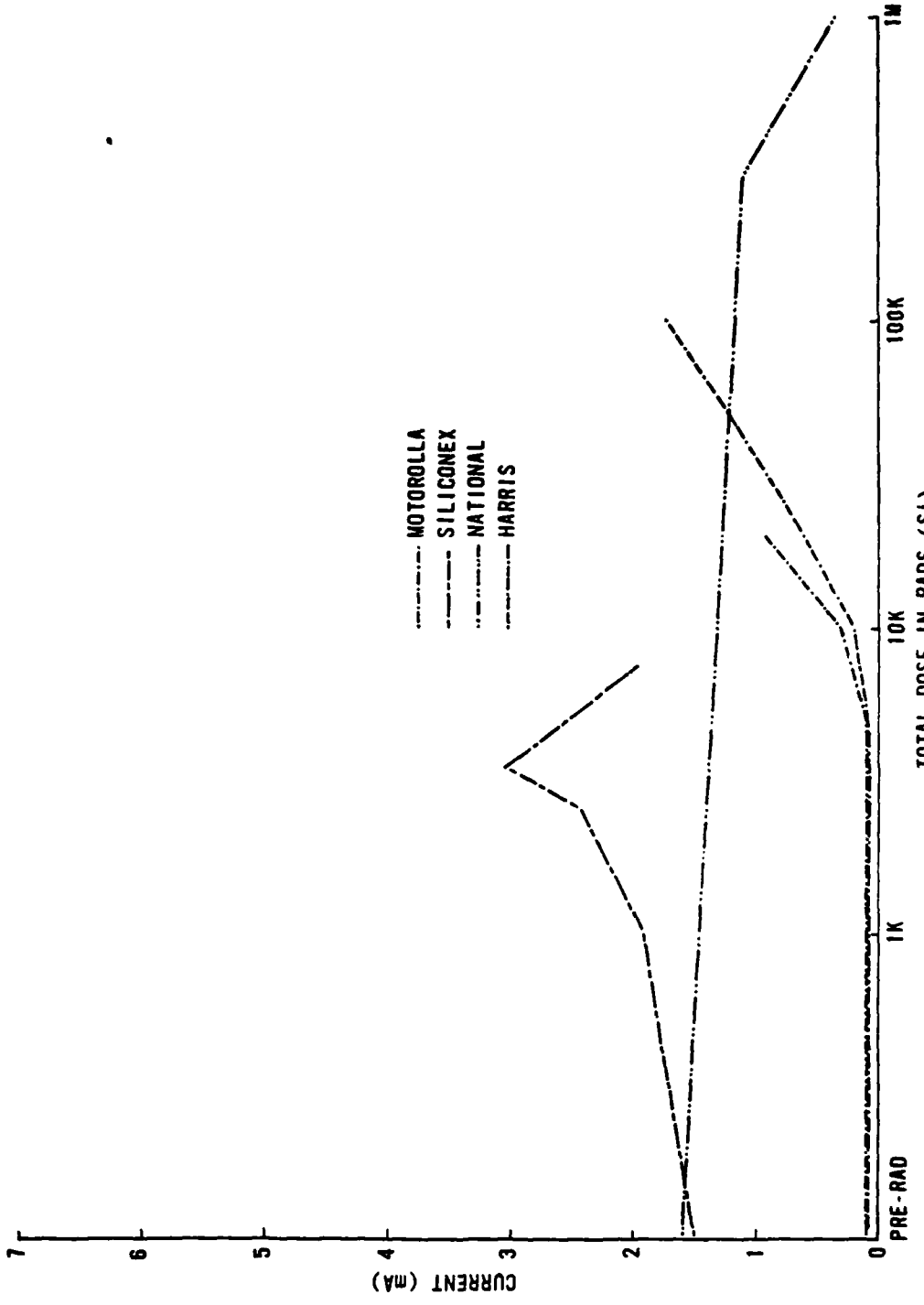


Figure 17. Negative standby supply current for devices irradiated while actively biased.

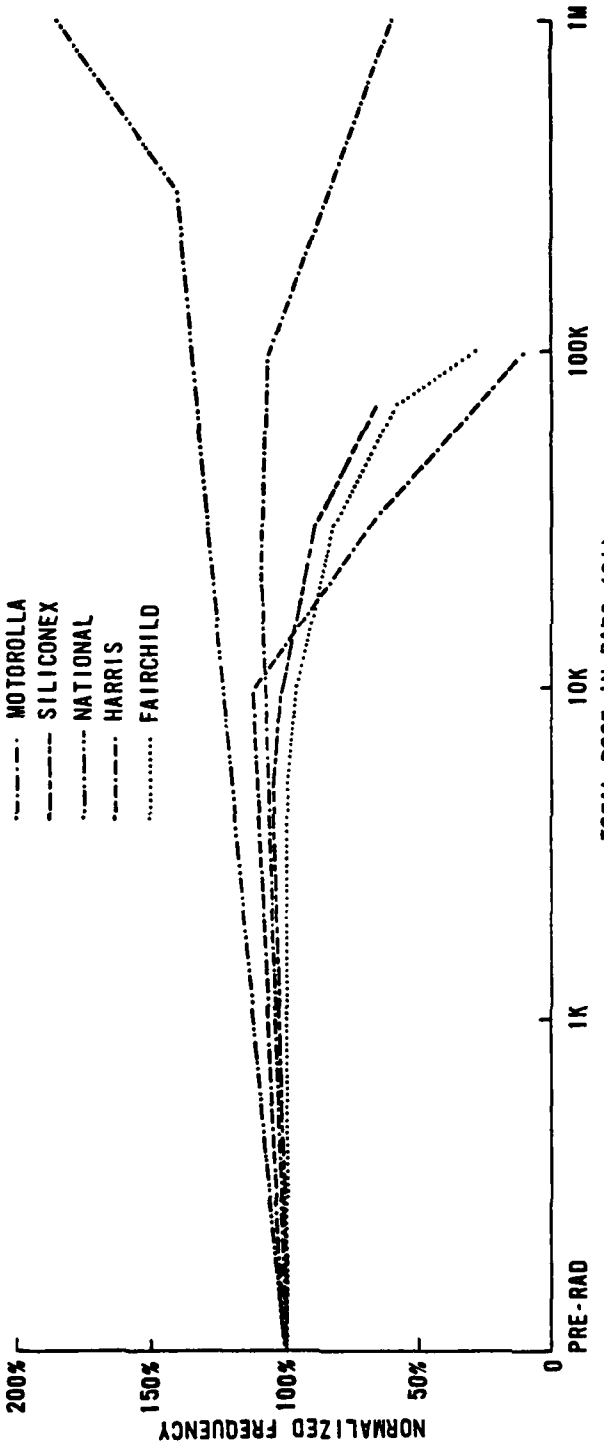


Figure 18. Normalized maximum digital control frequency for devices irradiated while grounded.

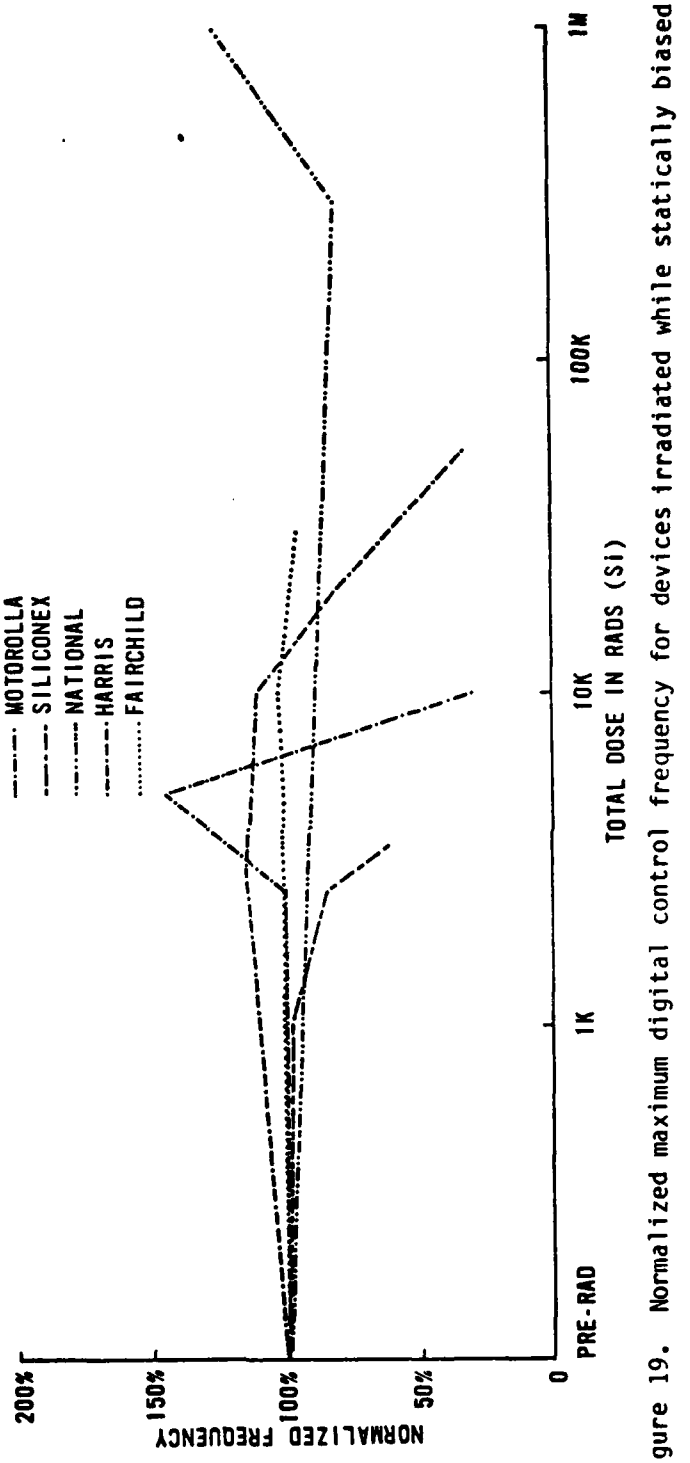


Figure 19. Normalized maximum digital control frequency for devices irradiated while statically biased.

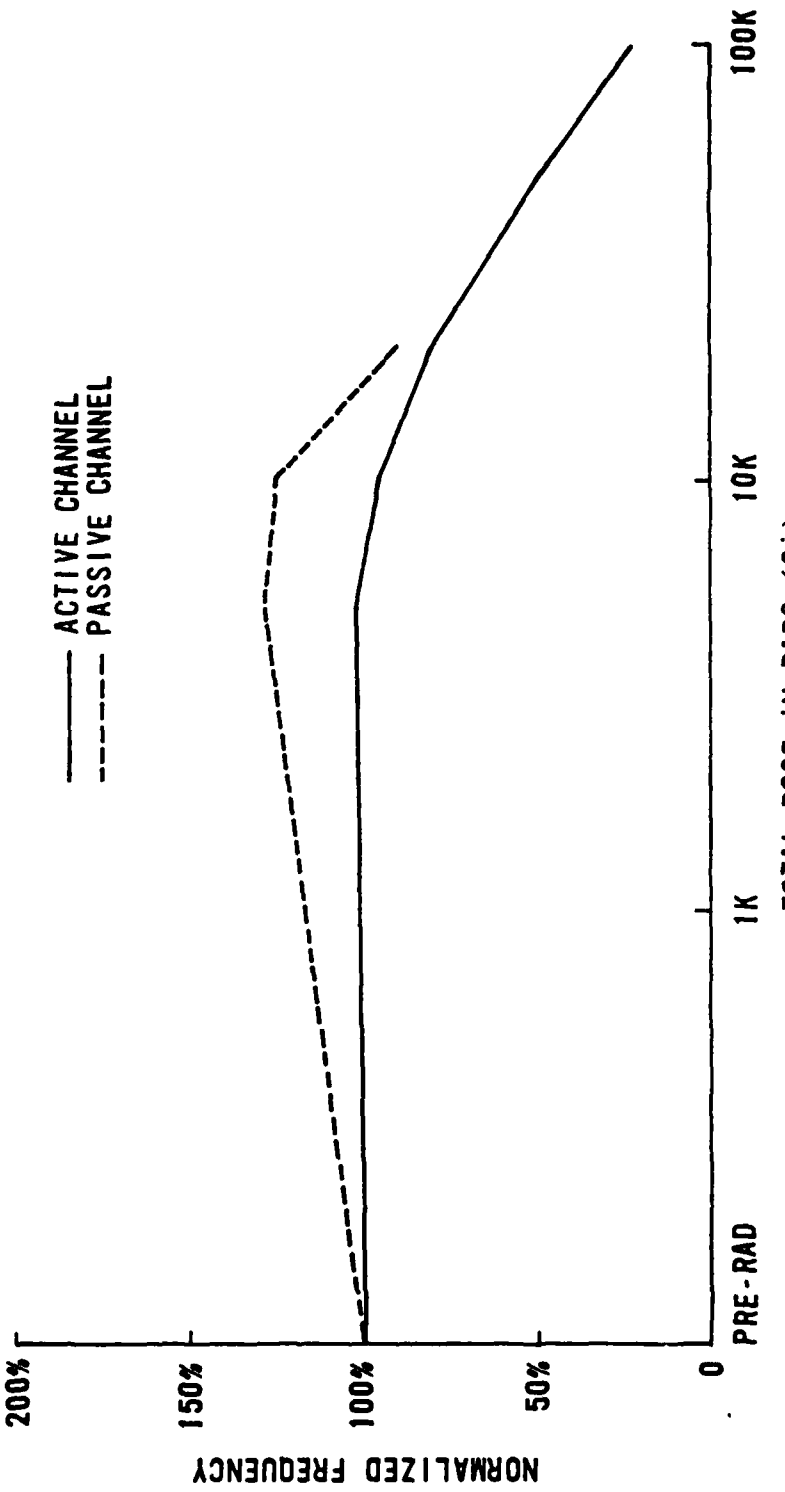


Figure 20. Normalized maximum digital control frequency for the Harris HI-506A-5 irradiated in an active mode.

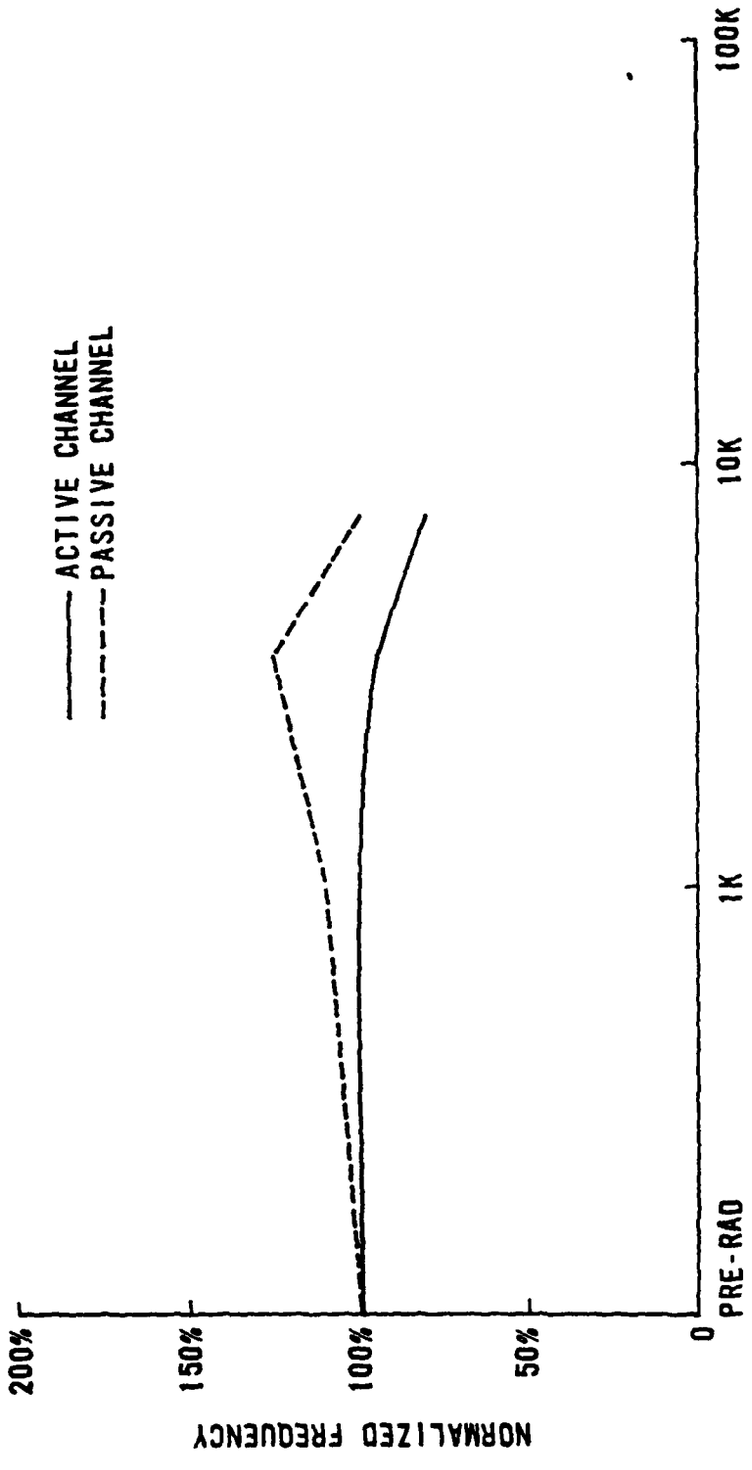


Figure 21. Normalized maximum digital control frequency for the Siliconex DG506 irradiated in an active mode.

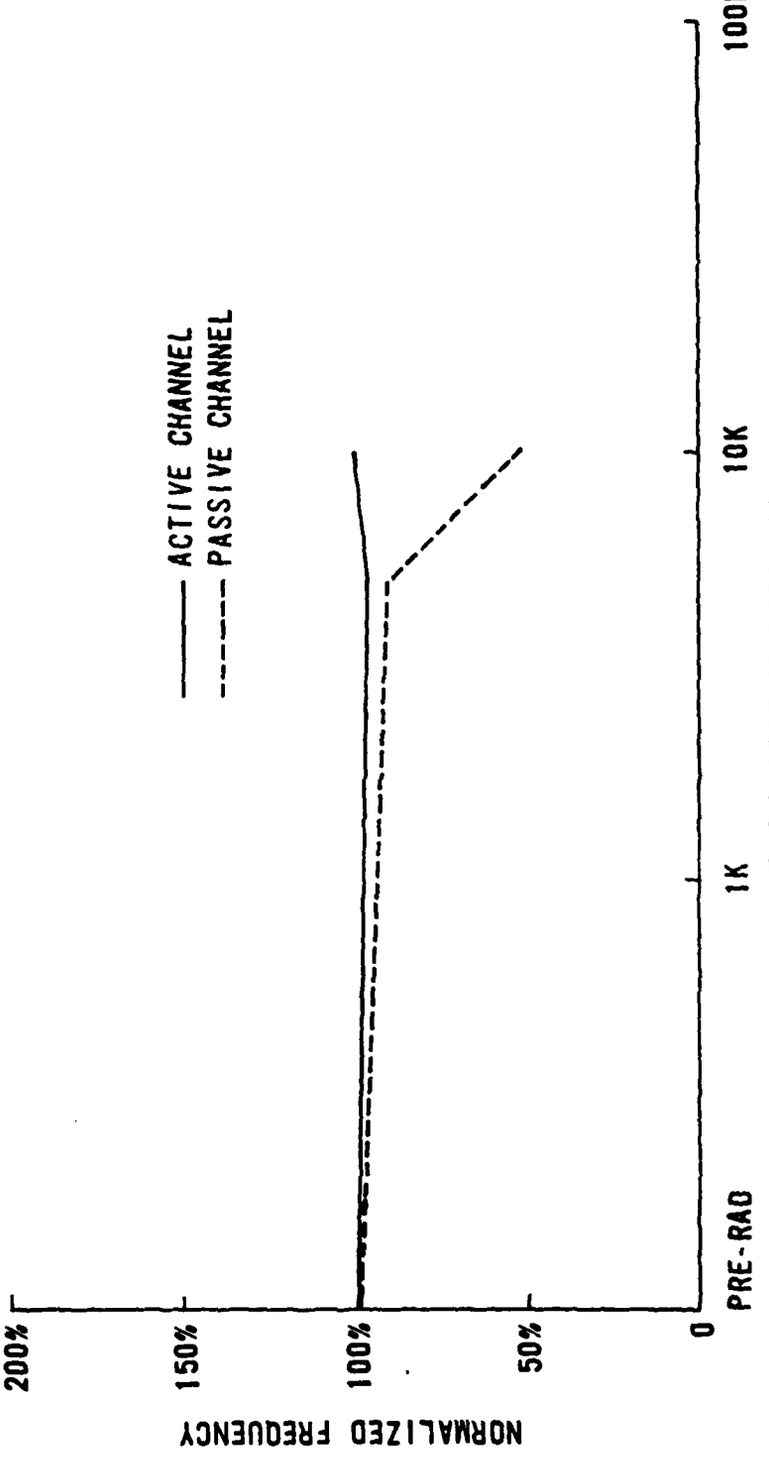


Figure 22. Normalized maximum digital control frequency for the Fairchild F4067B irradiated in an active mode.

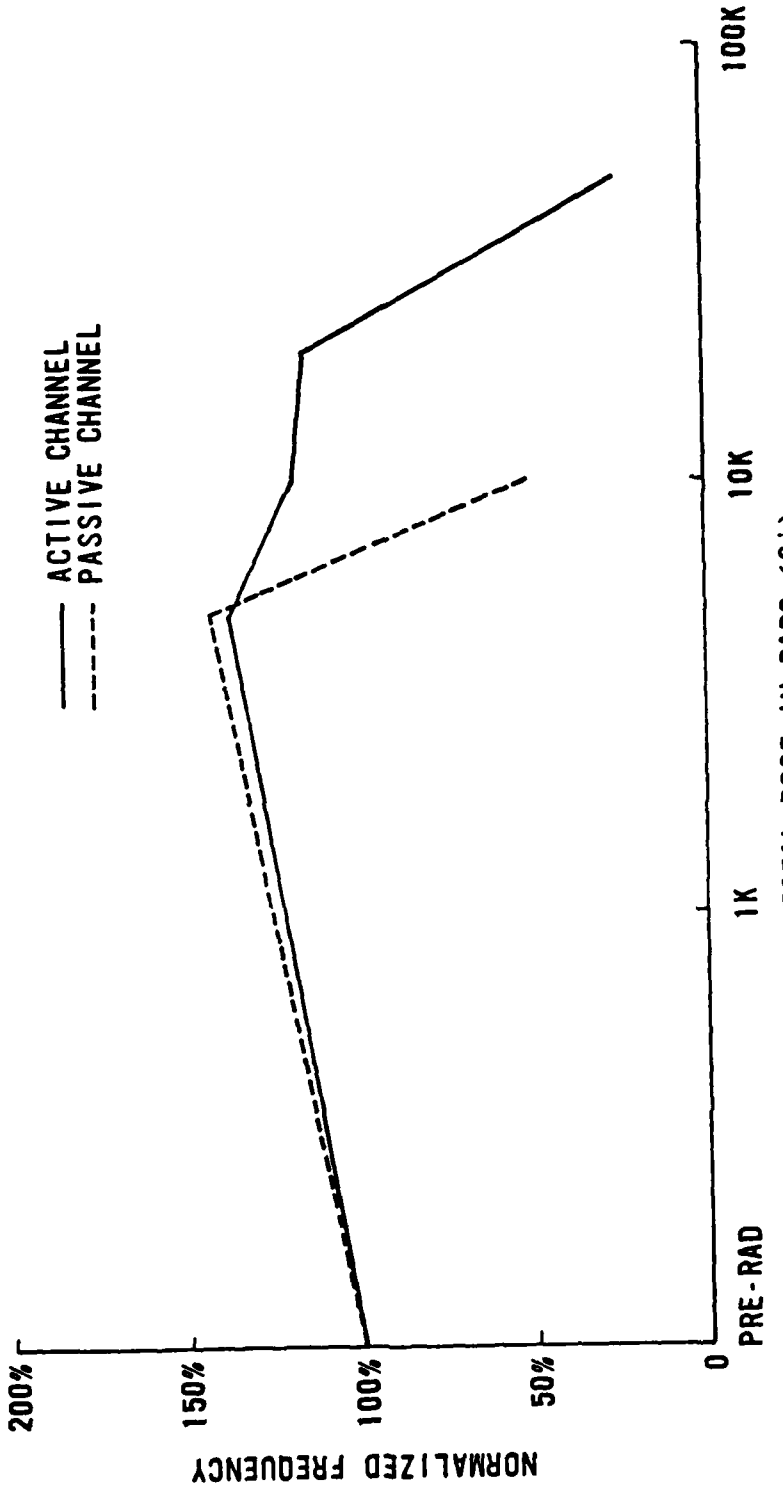


Figure 23. Normalized maximum digital control frequency for the Motorola MC14051 irradiated in an active mode.

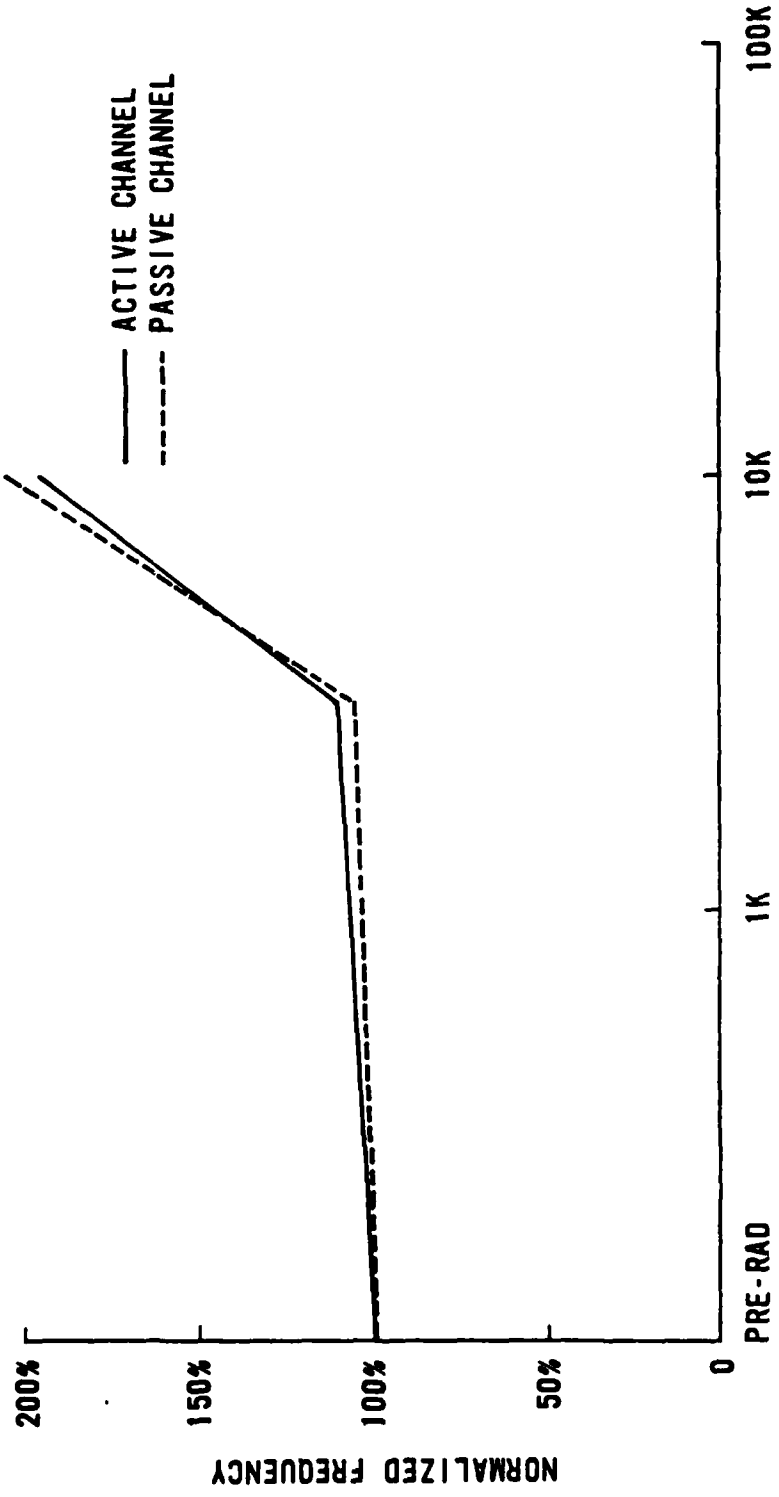


Figure 24. Normalized maximum digital control frequency for the National LF1508 irradiated in an active mode.